

Figure 1: Digital Delay Locked Loop Block Diagram with 4-bit Counter.

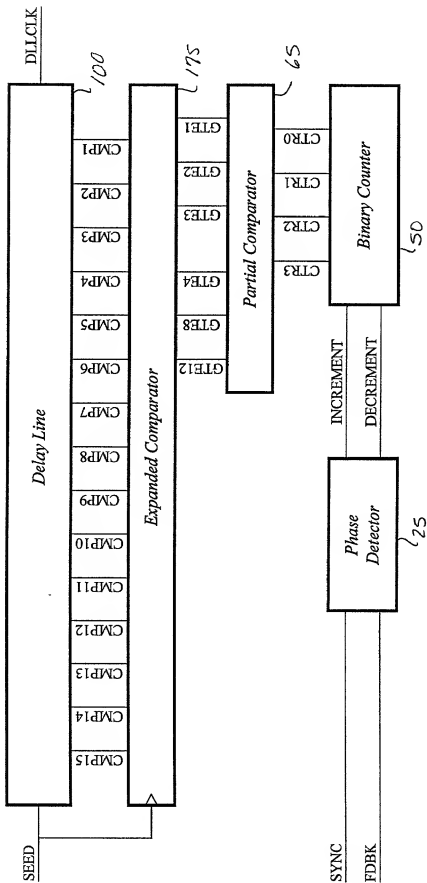


Figure 2: Digital Delay Locked Loop Block Diagram with 4-bit Counter and Partial Comparator.

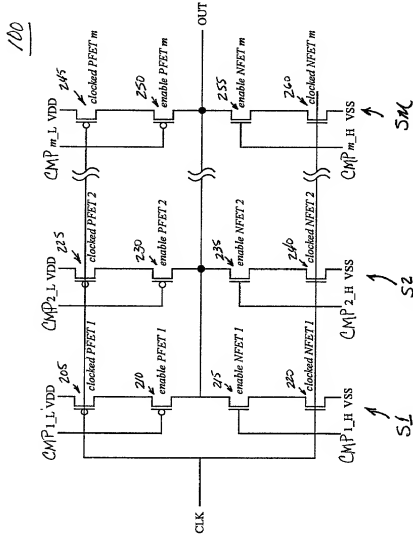


Figure 3: Delay Line Element with m Enable Inputs.

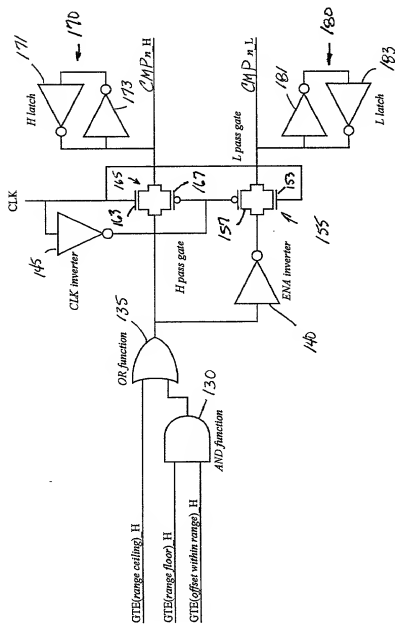


Figure 4: Element of Expanded Comparator.

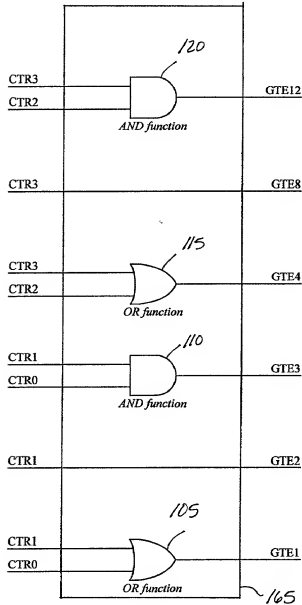


Figure 5: Partial Comparator for 4-bit Counter.

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Atty.'s Docket No. 1662-37600 (P00-3208)
 Applicant: Daniel William BAILEY
 Title: Expanded Comparator For Control Of Digital Delay Lines In
 A Delay Locked Loop Or Phase Locked Loop
 Sheet 6 of 6 Express Mail Label No. EV041361644US

INPUT				OUTPUT														
CTR3	CTR2	CTR1	CTR0	CMP1	CMP2	CMP3	CMP4	CMP5	CMP6	CMP7	CMP8	CMP9	CMP10	CMP11	CMP12	CMP13	CMP14	CMP15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6

Table 1: Truth Table for 4-to-15 bit Expanded Comparator.